Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1. A method for fabricating a buried bit line of a mask ROM, the method comprising:

providing a semiconductor substrate with a photoresist layer coated on the semiconductor substrate;

patterning the photoresist layer to form a photoresist pattern;

performing a first ion implantation process to form a first doped region in the semiconductor substrate not covered by the photoresist pattern;

forming an organic spacer on sidewall of the photoresist pattern;

performing a second ion implantation process to form a second doped region in the semiconductor substrate not covered by the photoresist pattern and the organic spacer; and

stripping the photoresist pattern and the organic spacer.

[c2] 2. The method of claim 1 further comprising performing a hot treatment process to harden the photoresist pattern after performing the first ion implantation process.

[c3] 3. The method of claim 2 wherein the hot treatment pro-

cess is an UV curing process or a hot plate process.

[c4] 4. The method of claim 1 wherein the first doped region is a lightly doped drain (LDD).

[c5] 5. The method of claim 1 wherein the second doped region is an N^+ doped region.

[c6] 6. The method of claim 1 wherein the organic layer is made of a bottom anti-reflective coating (BARC).

[c7] 7. The method of claim 1 wherein the step of forming the organic spacer includes a step of performing a dry etching process.

[c8] 8. A method for fabricating a mask ROM, the method comprising:
providing a semiconductor substrate with a photoresist layer coated on the semiconductor substrate;
patterning the photoresist layer to form a photoresist pattern;
performing a first ion implantation process to form a first doped region in the semiconductor substrate not covered by the photoresist pattern;
performing a hot treatment process to harden the photoresist pattern;
forming an organic spacer on sidewall of the photoresist pattern;

performing a second ion implantation process to form a second doped region in the semiconductor substrate not covered by the photoresist pattern and the organic spacer;

stripping the photoresist pattern and the organic spacer; and

forming an insulating layer on the semiconductor substrate and an word line on the insulating layer.

[c9] 9. The method of claim 8 wherein the hot treatment process is an UV curing process or a hot plate process.

[c10] 10. The method of claim 8 wherein the first doped region is a lightly doped drain (LDD).

[c11] 11. The method of claim 8 wherein the second doped region is an N^+ doped region.

[c12] 12. The method of claim 8 wherein the organic spacer is made of a bottom anti-reflective coating (BARC) material.

[c13] 13. The method of claim 8 wherein the step of forming the organic spacer includes a step of performing a dry etching process.